DEVICES HAVING PATTERNED REGIONS OF POLYCRYSTALLINE ORGANIC SEMICONDUCTORS, AND METHODS OF MAKING THE SAME

5   Field of the Invention

The present invention relates to organic semiconductor devices and circuits containing organic semiconductor devices.

Background of the Invention

10   Semiconductor devices are typically formed as multilayer structures in which the semiconductor materials are present in a patterned array that defines channels for the transport of charge carriers. For example, an inorganic semiconductor layer may be applied to a dielectric substrate surface. A mask may then be applied to protect patterned regions of the semiconductor layer, intended to constitute charge carrier channels, from a subsequently applied etchant. The

15   etchant then removes the semiconductor in the unmasked regions, leaving behind a finely patterned array of semiconductor channels on the substrate. In the absence of such patterning, the semiconductor devices may be inoperable or be subject to excessive crosstalk.

Inorganic semiconductors typically are rigid and brittle at ambient temperatures. Hence, semiconductor devices formed with inorganic semiconductors generally are rigid as well. As the

20   myriad end use applications for semiconductor devices have evolved, availability of semiconductor devices that can be flexed and bent without damage has become desirable. Flexible semiconductor device structures also offer a potential capability for fabrication of large area device arrays at low unit costs.

Much work has been done to develop organic semiconductors for applications where

25   flexible semiconductor devices are needed. However, organic semiconductors generally cannot survive the harsh conditions required in order to carry out an etching step to generate a patterned

array of channels for charge carrier transport. Printing processes have accordingly been sought in order to directly provide a patterned semiconductor channel array without a need to remove regions of a continuous layer of semiconductor material. However, in some cases the fine feature definition that is needed to generate microarrays of semiconductor channels has not been attained

5   with acceptable reproducibility by direct printing of organic semiconductors.

Tetracene, for example, is an organic semiconductor of great interest due to its high charge carrier mobility in a single crystal. Single plate-like crystals of tetracene having dimensions as large as 5 millimeters long, 5 millimeter wide, and 0.25 millimeter thick have been produced. For example, individual thin film field effect transistors comprising single tetracene

10   crystals have been made with high channel mobilities within a range of between about 0.1 centimeters squared per volt-second (cm^2/Vs) and about 1 cm^2/Vs, at room temperature. However, tetracene thin film field effect transistors in general have low mobilities and on/off current ratios, and their integration into a circuit may require further development. Furthermore, vacuum evaporation of tetracene leads to poorly defined and irregular boundaries between crystal

15   grains that leads to low mobility and makes such grains unusable in fabricating semiconductor devices such as transistors or arrays comprising transistors.

One effort to generate a patterned array of semiconductor film channels comprising an aromatic acene semiconductor involved the direct printing of a pentacene precursor, which was then converted into pentacene. See, for example, Dimitrakopoulos et al. U.S. Patent. No.

20   5,981,970, issued on November 9, 1999 and entitled, "Thin-film field-effect transistor with organic semiconductor requiring low operating voltages." See also, Afzali, A., Dimitrakopoulos, C. D., and Breen, T. L., "High-performance, solution-processed organic thin film transistors from a novel pentacene precursor," J. Am. Chem. Soc. 124 (30), pp. 8812-8813, July 31, 2002. The entireties of both of the foregoing documents are hereby incorporated herein in their entirety.

Another process for forming patterned organic semiconductor films is disclosed in Katz

U.S. Patent No. 6,403,397 issued on June 11, 2002, which is entitled "Process For Fabricating

Organic Semiconductor Device Involving Selective Patterning", the entirety of which is hereby

incorporated herein. This process involves treating a surface to selectively provide regions of

5   greater affinity and lesser affinity for either an organic semiconductor or an organic

semiconductor solution. When the organic semiconductor, or solution comprising the

semiconductor, was deposited on the treated surface, either the organic semiconductor or the

organic semiconductor solution dewetted from the lesser affinity regions or the resultant film

adhered only weakly to the lesser affinity regions such that selective removal was readily

10   performed. Even where such removal was not performed, the portions of the organic

semiconductor film on the greater affinity regions exhibited higher conductivity and better film

continuity relative to the other portions of the film.

There remains a need for semiconductor devices comprising organic semiconductors

having finely patterned regions of high charge carrier mobility. There further is a need for

15   methods of making semiconductor devices with organic semiconductors that are not easily

patterned.

Summary of the Invention

The present invention provides semiconductor apparatus in which patterned regions of a

20   polycrystalline aromatic organic semiconductor are grown on a substrate. The patterning is

directed by materials applied to the substrate to either promote or inhibit nucleation of crystals of

the organic semiconductor. The material that promotes nucleation of the aromatic semiconductor

comprises an aromatic moiety that can interact with the aromatic semiconductor. The exemplary

material that inhibits nucleation of the aromatic semiconductor comprises a non-aromatic moiety

or an aromatic moiety having insufficient conjugated pi-electrons to effectively interact with the aromatic semiconductor.

In one embodiment, a semiconductor apparatus is provided, comprising a substrate having a substrate surface; and a first dielectric layer comprising molecules of a first compound, the molecules of the first compound having first ends and second ends, the first ends being covalently bonded to a first region of the substrate surface, the second ends having aromatic regions. A polycrystalline semiconductor layer comprising organic semiconductor molecules with aromatic portions is also provided, the polycrystalline semiconductor layer being on the first region of the substrate.

In another embodiment, such a semiconductor apparatus is provided in which the organic semiconductor molecules comprise y conjugated pi-electrons, in which y is an integer of 10 or more, and the second ends of molecules of the first compound comprise at least y minus 8 conjugated pi-electrons.

In a further embodiment, such a semiconductor apparatus is provided comprising a second dielectric layer comprising molecules of a second compound, the molecules of the second compound having third ends and fourth ends, the third ends being covalently bonded to a second region of the substrate surface, the fourth ends comprising no more than y minus 8 conjugated pi-electrons.

In an additional embodiment, a method of making a semiconductor apparatus is provided, comprising the steps of providing a substrate having a substrate surface; and providing a first dielectric layer comprising molecules of a first compound, the molecules of the first compound having first ends and second ends, the first ends being covalently bonded to a first region of the substrate surface, the second ends having aromatic regions. Further, a polycrystalline semiconductor layer is provided comprising organic semiconductor molecules with aromatic portions, the polycrystalline semiconductor layer being on the first region of the substrate.

The present invention further provides methods of making such semiconductor apparatus. In further embodiments, integrated circuits comprising semiconductor apparatus and methods for making such integrated circuits are provided.

A more complete understanding of the present invention, as well as further features and advantages of the invention, will be apparent from the following detailed description and the accompanying drawings.

Brief Description of the Drawings

Fig. 1 shows a top view of an exemplary embodiment of two thin film transistors;

Fig. 2 shows a cross-sectional view of the exemplary embodiment of Fig. 1;

Fig. 3 shows a top view of another exemplary embodiment of two thin film transistors;

Fig. 4 shows a cross-sectional view of the exemplary embodiment of Fig. 3;

Fig. 5 shows a top view of a further exemplary embodiment of two thin film transistors;

Fig. 6 shows a cross-sectional view of the exemplary embodiment of Fig. 5;

Fig. 7 shows a flow chart for an exemplary method of making the thin film transistors shown in Figs. 1 and 2;

Fig. 8 shows a flow chart for an exemplary method of making the thin film transistors shown in Figs. 3 and 4; and

Fig. 9 shows a flow chart for an exemplary method of making the thin film transistors shown in Figs. 5 and 6.

Fig. 10 shows results of an experiment in which a substrate was stamped in a pattern with triphenylthiol and then soaked into mercaptododecane, prior to exposure to and selective nucleation of monochlorotetracene.

The drawings of this specification are not to scale but are merely schematic representations, and thus are not intended to portray the specific dimensions of the various embodiments.

5   Detailed Description

Embodiments will now be described more fully with reference to the accompanying drawings. This invention may, however, be embodied in various forms and should not be construed as being limited to the embodiments set forth herein.

Semiconductor apparatus are provided in which patterned regions of a polycrystalline

10   aromatic organic semiconductor are grown on a substrate. The patterning is directed by materials applied to the substrate to either promote or inhibit nucleation of crystals of the organic semiconductor. The material that promotes nucleation of the aromatic semiconductor comprises an aromatic moiety that can interact with the aromatic semiconductor. In exemplary embodiments the material that inhibits nucleation of the aromatic semiconductor comprises a

15   non-aromatic moiety or an aromatic moiety having insufficient conjugated pi-electrons, that can interact with the aromatic semiconductor.

Fig. 1 shows an exemplary embodiment 100 of two thin film transistors generally indicated at 102 and 104. Thin film transistor 102 comprises a source electrode 106 and a drain electrode 108 in a spaced apart arrangement on a dielectric layer 110. The source electrode 106

20   and drain electrode 108 are fabricated from a composition to which a thiol moiety can bond, such as a composition comprising gold, silver, platinum, palladium, copper, or alloys of such elements. Thin film transistor 104 comprises a source electrode 112 and a drain electrode 114 fabricated from the same materials in a spaced apart arrangement on dielectric layer 110. A surface of each of the source electrodes 106 and 112 and of the drain electrodes 108 and 114 is

25   centrally provided with semiconductor crystal nucleation augmentation regions 116, 120, 118

and 122, respectively constituted by a coating composition comprising a compound having a

thiol moiety the electrodes and an aromatic moiety positioned to interact with a subsequently

applied aromatic semiconductor. The aromatic moiety is so positioned because it is not bonded

to the electrodes, whereas the thiol moiety is bonded to one of the electrodes. The surface of

5 each of the source electrodes 106 and 112 and of the drain electrodes 108 and 114 is at each end

further provided with semiconductor crystal nucleation inhibition regions 124 and 126, 132 and

134, 128 and 130, and 136 and 138 respectively constituted by a coating composition comprising

a compound having a thiol moiety that can bond to the electrodes and a non-aromatic moiety

positioned to interact with a subsequently applied aromatic semiconductor. The non-aromatic

10 moiety is so positioned because it is not bonded to the electrodes, whereas the thiol moiety is

bonded to one of the electrodes. Polycrystalline semiconductor layer 140 is on the dielectric

layer 110 and on semiconductor nucleation augmentation regions 116 and 118, forming a channel

region of transistor 102 having a high charge carrier mobility. Polycrystalline semiconductor

layer 142 is on the dielectric layer 110 and on semiconductor nucleation augmentation regions

15 120 and 122, forming a channel region of transistor 104 having a high charge carrier mobility.

The polycrystalline semiconductor layers 140 and 142 are formed by interaction of the

semiconductor with the aromatic moieties of semiconductor crystal nucleation augmentation

regions 116-122 upon semiconductor application.

 Fig. 2 shows a cross-sectional view of the exemplary embodiment 100 of thin film

20 transistors 102 and 104, taken on line 2-2 in Fig. 1. Source electrodes 106 and 112, and drain

electrodes 108 and 114, are supported on dielectric layer 110. Dielectric layer 110 is supported

on a gate electrode 144. The gate electrode 144 is supported on a supporting substrate 146.

Semiconductor crystal nucleation augmentation region 116 of source electrode 106,

semiconductor crystal nucleation augmentation region 118 of drain electrode 108, semiconductor

25 crystal nucleation augmentation region 120 of source electrode 112, and semiconductor crystal

nucleation augmentation region 122 of drain electrode 114, each is constituted by a coating composition comprising an aromatic moiety. Semiconductor layer 140 is on source electrode 106, drain electrode 108, and dielectric layer 110. Semiconductor layer 142 is on source electrode 112, drain electrode 114, and dielectric layer 110. The source electrodes 106 and 112,

5   drain electrodes 108 and 114, and gate electrode 144 are in communication with an electrical circuit, not shown, of which thin film transistors 102 and 104 form a part.

Referring to Fig. 2, semiconductor crystal nucleation augmentation regions 116-122 are formed of dielectric materials that promote nucleation of the selected semiconductor, resulting in formation of semiconductor layers 140 and 142, respectively. If the semiconductor crystal

10   nucleation augmentation regions 116-122 are too thick, injection of a charge into the semiconductor layers 140 and 142 may be difficult. Therefore, desirably in one embodiment, semiconductor crystal nucleation augmentation regions 116-122 have a thickness t that is no greater than about 5 nanometers. The semiconductor crystal nucleation augmentation regions 116-122 promote formation of semiconductor crystal nuclei on their surfaces, which then grow

15   together forming semiconductor layers 140 and 142 constituting channel regions for the transistors 102 and 104. At the same time, semiconductor nucleation inhibition regions 124-138 allow substantially less or virtually no nucleation of the selected semiconductor. In one embodiment, the semiconductor nucleation inhibition regions 124-138 are omitted. However, such omission may permit the random nucleation of semiconductor crystals on the electrodes. In

20   another embodiment, the electrodes 106, 108, 112, and 114 are embedded in the dielectric layer 110 so that the semiconductor layers 140 and 142 are substantially flush with the surface 111 of the dielectric layer 110. The electrodes 106, 108, 112, and 114 can be so embedded by etching the dielectric layer 110 prior to their deposition.

In operation of the exemplary thin film transistor 102, a voltage applied to the gate

25   electrode 144 can be used to control a flow of charge carriers between the source electrode 106

and the drain electrode 108. Similarly, in operation of the exemplary thin film transistor 104, a voltage applied to the gate electrode 144 can be used to control a flow of charge carriers between the source electrode 112 and the drain electrode 114. The portion of the gate electrode 144 underlying exemplary thin film transistor 102 may be separated and electrically isolated from the portion of the gate electrode 144 underlying exemplary thin film transistor 104. In thin film transistor 102, charge carriers are transported between the source electrode 106 and the drain electrode 108 through the semiconductor layer 140. Similarly in thin film transistor 104, charge carriers are transported between the source electrode 112 and the drain electrode 114 through the semiconductor layer 142.

Fig. 3 shows an exemplary embodiment 300 of two thin film transistors generally indicated at 302 and 304. Thin film transistor 302 comprises a source electrode 306 and a drain electrode 308 in a spaced apart arrangement on a dielectric layer 310. Thin film transistor 304 comprises a source electrode 312 and a drain electrode 314 in a spaced apart arrangement on dielectric layer 310. Dielectric layer 310 is fabricated from a material comprising silicon, such as SiO_2 or an alkyl siloxane. Siloxanes are compounds that have the general formula $SiOR_1R_2R_3$, in which R_1, R_2, and R_3 can each independently be selected from the group consisting of: Cl, -O-CH_3, -O-CH_2CH_3, or R in which R is a hydrocarbon moiety such as an alkyl group for example. Background information regarding such dielectric layers is provided in Collet, J., et al., "High Anisotropic Conductivity in Organic Insulator / Semiconductor Monolayer Heterostructure," Applied Physics Letters, Vol. 76, No. 10, pp. 1339-1341, March 6, 2000, the entirety of which is hereby incorporated herein by reference.

A portion of the dielectric layer 310 that is centrally located between the source electrode 306 and the drain electrode 308 of transistor 302 is provided with semiconductor crystal nucleation augmentation region 316 thereon, constituted by a coating of a composition comprising aromatic moieties and comprising moieties containing reactive silicon atoms, such as

$SiCl_3$ groups or $SiOR_3$ groups. A portion of the dielectric layer 310 that is centrally located

between the source electrode 312 and the drain electrode 314 of transistor 304 is provided with

semiconductor crystal nucleation augmentation region 318 thereon, also constituted by a coating

of a composition comprising aromatic moieties and comprising moieties containing reactive

5   silicon moieties, such as $SiCl_3$ groups or $SiOR_3$ groups. The moieties of such coatings that

comprise reactive silicon atoms, such as $SiCl_3$ groups or $SiOR_3$ groups, are chemically attracted

to and become juxtaposed to the silicon in dielectric layer 310. The aromatic moieties of such

coatings are not so attracted and accordingly become positioned facing away from the dielectric

layer 310. If the semiconductor crystal nucleation augmentation regions 316 and 318 are too

10   thick, injection of a charge into the respective semiconductor layers 326 and 328 may be

difficult. Therefore, desirably in one embodiment, semiconductor crystal nucleation

augmentation regions 316 and 318 have a thickness h that is no greater than about 5 nanometers.

The portion of the dielectric layer 310 excluding the semiconductor crystal nucleation

augmentation regions 316 and 318 is provided with a coextensive semiconductor crystal

15   nucleation inhibition region 320 constituted by a coating of a composition comprising non-

aromatic moieties and comprising moieties containing reactive silicon atoms, such as $SiCl_3$

groups or $SiOR_3$ groups. The moieties of such coatings that comprise reactive silicon atoms,

such as $SiCl_3$ groups or $SiOR_3$ groups, are chemically attracted to and become juxtaposed to the

silicon in dielectric layer 310. The non-aromatic moieties of such coatings are not so attracted

20   and accordingly become positioned facing away from the dielectric layer 310. Together, the

regions 316, 318 and 320 define a patterned coating on the dielectric substrate 310, in which a

coating comprising aromatic groups is only provided in the semiconductor crystal nucleation

augmentation regions 316 and 318. A polycrystalline semiconductor is on the semiconductor

crystal nucleation augmentation regions 316 and 318 of transistors 302 and 304, respectively, and

makes contact with the source and drain electrodes forming channel regions having a high charge

carrier mobility.

Fig. 4 shows a cross-sectional view of the exemplary embodiment 300 of thin film

transistors 302 and 304, taken on line 4-4 in Fig. 3. Source electrodes 306 and 312, and drain

5   electrodes 308 and 314 are supported on dielectric layer 310. Dielectric layer 310 is supported

on a gate electrode 322. The gate electrode 322 is supported on a supporting substrate 324.

Semiconductor crystal nucleation augmentation regions 316 and 318 of transistors 302 and 304,

respectively, are supported on the dielectric layer 310 and constituted by coatings of a

composition comprising aromatic moieties and comprising moieties containing reactive silicon

10   atoms, such as $SiCl_3$ groups or $SiOR_3$ groups. A semiconductor layer 326 is in contact with

source electrode 306, drain electrode 308, and is on the semiconductor crystal nucleation

augmentation region 316. A semiconductor layer 328 is in contact with source electrode 312,

drain electrode 314, and is on semiconductor crystal nucleation augmentation region 318.

Semiconductor crystal nucleation inhibition regions 330, 332 and 334 collectively form the

15   semiconductor nucleation inhibition region 320 on the dielectric layer 310 and are constituted by

coatings of a composition comprising non-aromatic moieties and comprising moieties containing

reactive silicon atoms, such as $SiCl_3$ groups or $SiOR_3$ groups. The source electrodes 306 and

312, drain electrodes 308 and 314, and gate electrode 322 are in communication with an

electrical circuit, not shown, of which thin film transistors 302 and 304 form a part. In another

20   embodiment, the electrodes 306, 308, 312 and 314 are embedded in the dielectric layer 310 so

that the semiconductor layers 326 and 328 are substantially flush with the surface 311 of the

dielectric layer 310.

Referring to Fig. 4, semiconductor crystal nucleation augmentation regions 316 and 318

are formed of dielectric materials comprising aromatic moieties that promote nucleation of the

25   selected aromatic organic semiconductor, forming semiconductor regions 326 and 328

constituting channel regions for the transistors 302 and 304. At the same time, semiconductor

nucleation inhibition region 320 constituted by semiconductor crystal nucleation inhibition

regions 330, 332 and 334, allows substantially less or virtually no nucleation of the selected

aromatic organic semiconductor. In one embodiment, the semiconductor nucleation inhibition

5 region 320 is omitted. However, such omission may permit the random nucleation of

semiconductor crystals on the dielectric substrate 310.

In another embodiment, a surface of each of the source electrodes 106 and 112 and of the

drain electrodes 108 and 114 shown in Fig. 4 is centrally provided, as discussed above in

connection with Figs. 1 and 2, with semiconductor crystal nucleation augmentation regions 116,

10 118, 120 and 122, constituted by coatings of a composition comprising a thiol moiety that can

bond to the electrodes and an aromatic moiety positioned to interact with a subsequently applied

aromatic semiconductor. Further as discussed above in connection with Figs. 1 and 2, the surface

of each of the source electrodes 106 and 112 and of the drain electrodes 108 and 114 is at each

end further provided with semiconductor crystal nucleation inhibition regions 124 and 126, 132

15 and 134, 128 and 130, and 136 and 138, constituted by a coating of a composition comprising a

thiol moiety that can bond to the electrodes and a non-aromatic moiety positioned to interact with

a subsequently applied aromatic semiconductor. In this manner, the semiconductor crystal

nucleation augmentation regions 316 and 318 shown in Fig. 3, and the semiconductor crystal

nucleation augmentation regions 116, 118, 120 and 122 shown in Fig. 1, collectively constitute a

20 patterned region that promotes nucleation of crystals of the aromatic organic semiconductor.

Further, the semiconductor crystal nucleation inhibition region 320 shown in Fig. 3, and the

semiconductor crystal nucleation inhibition regions 124-138 shown in Fig. 1, collectively

constitute a patterned region that inhibits nucleation of crystals of the aromatic organic

semiconductor.

In operation of the exemplary thin film transistor 302, a voltage applied to the gate electrode 322 can be used to control a flow of charge carriers between the source electrode 306 and the drain electrode 308. Similarly, in operation of the exemplary thin film transistor 304, a voltage applied to the gate electrode 322 can be used to control a flow of charge carriers between

5   the source electrode 312 and the drain electrode 314. The portion of the gate electrode 322 underlying exemplary thin film transistor 302 may be separated and electrically isolated from the portion of the gate electrode 322 underlying exemplary thin film transistor 304. In thin film transistor 302, charge carriers are transported between the source electrode 306 and the drain electrode 308 through the semiconductor layer 326. Similarly in thin film transistor 304, charge

10   carriers are transported between the source electrode 312 and the drain electrode 314 through the semiconductor layer 328.

Fig. 5 shows an exemplary embodiment 500 of two thin film transistors generally indicated at 502 and 504. Thin film transistor 502 comprises a source electrode 506 and a drain electrode 508 in a spaced apart arrangement on a semiconductor layer 510. Thin film transistor

15   504 comprises a source electrode 512 and a drain electrode 514 in a spaced apart arrangement on a semiconductor layer 516. Transistors 502 and 504 are supported by a dielectric layer 518 fabricated from a material comprising silicon, such as SiO_2 or a siloxane.

Fig. 6 shows a cross-sectional view of the exemplary embodiment 500 of thin film transistors 502 and 504, taken on line 6-6 in Fig. 5. Source electrode 506 and drain electrode 508

20   of transistor 502 are on semiconductor layer 510. Source electrode 512 and drain electrode 514 of transistor 504 are on semiconductor layer 516. Semiconductor layer 510 is on semiconductor crystal nucleation augmentation region 520, such augmentation region constituted by a coating of a composition comprising aromatic moieties and comprising moieties containing reactive silicon atoms, such as $SiCl_3$ groups or $SiOR_3$ groups. Semiconductor layer 516 is on semiconductor

25   crystal nucleation augmentation region 522, such augmentation region being constituted by a

coating of a composition comprising aromatic moieties and comprising moieties containing reactive silicon atoms, such as $SiCl_3$ groups or $SiOR_3$ groups. The semiconductor crystal nucleation augmentation regions 520 and 522 are on dielectric layer 518. The moieties of the coatings that comprise reactive silicon atoms, such as $SiCl_3$ groups or $SiOR_3$ groups, are

5   chemically attracted to and become juxtaposed to the silicon in dielectric layer 518. The aromatic moieties of the coatings are not so attracted and accordingly become positioned facing away from the dielectric layer 518. If the semiconductor crystal nucleation augmentation regions 520 and 522 are too thick, injection of a charge into the semiconductor layers 510 and 516 may be difficult. Therefore, desirably in one embodiment, semiconductor crystal nucleation

10   augmentation regions 520 and 522 have a thickness d that is no greater than about 5 nanometers.

Surrounding the semiconductor crystal nucleation augmentation regions 520 and 522 are semiconductor crystal nucleation inhibition regions 524, 526 and 528, constituted by a coating comprising non-aromatic moieties and comprising moieties containing reactive silicon atoms, such as $SiCl_3$ groups or $SiOR_3$ groups. The moieties of such coating that comprise reactive

15   silicon atoms, such as $SiCl_3$ groups or $SiOR_3$ groups, are chemically attracted to and become juxtaposed to the silicon in dielectric layer 518. The non-aromatic moieties of such coatings are not so attracted and accordingly become positioned facing away from the dielectric layer 518. Semiconductor crystal nucleation inhibition regions 524, 526 and 528 collectively form a semiconductor crystal nucleation inhibition region 530 shown in Fig. 5 on those portions of

20   dielectric layer 518 not supporting the semiconductor crystal nucleation augmentation regions 520 and 522. Together, the regions 520, 522, 524, 526, and 528 define a patterned coating on the dielectric substrate 518, in which a coating comprising aromatic groups is only provided in the semiconductor crystal nucleation augmentation regions 520 and 522. The semiconductor crystal nucleation augmentation regions 520 and 522 promote formation of semiconductor crystal nuclei

25   on their surfaces. At the same time, semiconductor nucleation inhibition region 530 allows

substantially less or virtually no nucleation of the selected aromatic organic semiconductor to occur. The semiconductor layer 510 on the semiconductor crystal nucleation augmentation region 520 makes contact with the source electrode 506 and the drain electrode 508, forming a channel region having a high charge carrier mobility. The semiconductor layer 516 on the

5 semiconductor crystal nucleation augmentation region 522 makes contact with the source electrode 512 and the drain electrode 514, forming a channel region having a high charge carrier mobility. In one embodiment, the semiconductor nucleation inhibition region 530 is omitted. However, such omission may permit the random nucleation of semiconductor crystals on the dielectric substrate 518. Dielectric layer 518 is supported on a gate electrode 532. The gate

10 electrode 532 is supported on a supporting substrate 534. The source electrodes 506 and 512, drain electrodes 508 and 514, and gate electrode 532 are in communication with an electrical circuit, not shown, of which thin film transistors 502 and 504 form a part.

In operation of the exemplary thin film transistor 502, a voltage applied to the gate electrode 532 can be used to control a flow of charge carriers between the source electrode 506

15 and the drain electrode 508. Similarly, in operation of the exemplary thin film transistor 504, a voltage applied to the gate electrode 532 can be used to control a flow of charge carriers between the source electrode 512 and the drain electrode 514. The portion of the gate electrode 532 underlying exemplary thin film transistor 502 may be separated and electrically isolated from the portion of the gate electrode 532 underlying exemplary thin film transistor 504. In thin film

20 transistor 502, charge carriers are transported between the source electrode 506 and the drain electrode 508 through the semiconductor layer 510. Similarly in thin film transistor 504, charge carriers are transported between the source electrode 512 and the drain electrode 514 through the semiconductor layer 516.

Figs. 1-6 as discussed above relate to exemplary and non-limiting embodiments. For

25 example, the embodiments shown in Figs. 1-6 each show two thin film transistors. Other

embodiments can comprise any desired quantity of thin film transistors. For example, the thin film transistors can be incorporated into an integrated circuit. Other designs for thin film transistors can be employed.

Further embodiments according to the invention will be discussed below in connection with thin film transistors. However, it is to be understood that the teachings herein can be further extended to devices other than thin film transistors that require lateral patterning of a semiconductor into discrete regions. For example, diodes can be produced in an analogous manner. Other exemplary semiconductor electronic devices that can be fabricated by use of the teachings herein include light emitting devices, photodetecting devices, photovoltaic cells, photoconductive cells, photoresistive cells, photodiodes, and photoswitches.

Appropriate compositions for forming coatings to constitute semiconductor crystal nucleation augmentation regions and semiconductor nucleation inhibition regions to be employed in making thin film transistors are selected depending upon the composition of the aromatic organic semiconductor to be employed and the composition of the substrate on which they are to be deposited. In one embodiment, coatings are applied to source and drain electrodes fabricated from a composition comprising gold, silver, platinum, palladium, copper, or alloys of such elements. Thiol compounds form strong bonds to these elements. Hence, the composition can be provided with thiol groups to facilitate both the bonding of the composition to the source and drain electrodes, and to facilitate orientation of the other moieties of the composition away from the surfaces of the source and drain electrodes where they can interact with a subsequently applied aromatic organic semiconductor. In another embodiment, coatings are applied to a dielectric layer comprising silicon, such as SiO_2 or a siloxane. Such a dielectric layer is susceptible to interaction with moieties containing reactive silicon atoms, such as $SiCl_3$ groups or $SiOR_3$ groups. R can be, for example, methyl or ethyl. Hence, the composition can be provided with moieties containing $SiCl_3$ groups or $SiOR_3$ groups to facilitate both the bonding of the

composition to the source and drain electrodes, and to facilitate orientation of the other moieties

of the composition away from the surfaces of the source and drain electrodes where they can

interact with a subsequently applied aromatic organic semiconductor. The composition of the

aromatic organic semiconductor to be used is taken into account in selecting the structure of the

5   moieties of the coating compositions intended to interact with the subsequently applied aromatic

organic semiconductor. The composition for forming coatings to constitute semiconductor

crystal nucleation augmentation regions further comprises aromatic moieties, which when

oriented away from the coating substrate are able to interact with and promote nucleation of the

subsequently applied aromatic semiconductor. In one embodiment, such aromatic moieties are

10   selected to have a number of conjugated aromatic pi-electrons that is at least as large as the same

number of conjugated aromatic pi-electrons present in the selected aromatic semiconductor

minus eight such pi-electrons (hereinafter an "influential amount" of pi-electrons). In another

embodiment, such aromatic moieties are selected to have a number of conjugated aromatic pi-

electrons that is an influential amount at least as large as the same number of conjugated aromatic

15   pi-electrons present in the selected aromatic semiconductor minus two such pi-electrons. The

composition for forming coatings to constitute semiconductor crystal nucleation inhibition

regions further comprises non-aromatic moieties, which when oriented away from the coating

substrate are able to interact with and inhibit nucleation of the subsequently applied aromatic

semiconductor. Alternatively, the composition for forming coatings to constitute semiconductor

20   crystal nucleation inhibition regions further comprises a number of conjugated aromatic pi-

electrons that is no greater than the same number of conjugated aromatic pi-electrons present in

the selected aromatic semiconductor minus eight such pi-electrons (hereinafter a "non-influential

amount" of pi-electrons).

In embodiments where thiol compounds are used, the thiol group forms a covalent bond

25   to the electrodes fabricated from gold, silver, platinum, palladium, copper, or an alloy. Hence, if

the molecules of the compound are placed in patterned contact with the gold electrode, they will orient themselves with the thiol moieties facing the gold electrode and then form covalent thio bonds anchoring the molecules in the desired pattern to the gold electrode. The position of such thiol groups on the compound can be selected to maximize the effectiveness of the resulting

5   semiconductor crystal nucleation augmentation and inhibition regions. For example, the thiol groups can be located at an extreme end of a longitudinal axis of molecules of the compound, so that the resulting bound molecules are oriented perpendicular to the surface of the electrode. In this manner, a highly ordered self-assembled monolayer of molecules of the compound can be prepared on patterned regions of the electrode. Compounds having multiple thiol groups are less

10   preferred for use with regard to preparing semiconductor crystal nucleation augmentation regions, as the resulting multiple bonding sites between the molecules and the gold electrode degrade the ordered assembly of the monolayer and of the resulting nucleation sites for the aromatic organic semiconductor.

In embodiments where compounds containing reactive silicon atoms, such as $SiCl_3$

15   groups or $SiOR_3$ groups are used, the silicon-containing group forms a covalent bond to the dielectric layer comprising silicon. Hence, if the molecules of the compound are placed in patterned contact with the dielectric layer, they will orient themselves with the silicon-containing moieties facing the dielectric substrate and then form covalent bonds anchoring the molecules in the desired pattern to the dielectric substrate. The position of such silicon-containing groups on

20   the compound can be selected to maximize the effectiveness of the resulting semiconductor crystal nucleation augmentation and inhibition regions. For example, the silicon-containing groups can be located at an extreme end of a longitudinal axis of molecules of the compound, so that the resulting bound molecules are oriented perpendicular to the surface of the electrode. In this manner, a highly ordered self-assembled monolayer of molecules of the compound can be

25   prepared on patterned regions of the electrode. Compounds having multiple silicon-containing

groups are less preferred for use with regard to preparing semiconductor crystal nucleation augmentation regions, as the resulting multiple bonding sites between the molecules and the dielectric substrate degrade the ordered assembly of the monolayer and of the resulting nucleation sites for the aromatic organic semiconductor.

5   Once nucleation of the semiconductor is established on the substrate surface, semiconductor crystals can then grow from the semiconductor nuclei. As a result, discrete polycrystalline semiconductor regions generally grow in a patterned array as desired, separated by regions that are either substantially devoid of semiconductor deposits, or that are characterized by relatively small and isolated crystals. In this manner, an aromatic organic semiconductor can

10   be applied to the substrate in a desired pattern to form thin film transistors.

For an exemplary p-type semiconductor capable of transporting holes, electrical conductivity is approximated by the formula $\sigma = en\mu_d$ where μ_d is the carrier mobility, e is the charge on the carriers, and n is the density of free carriers. Conductivity accordingly is proportional to mobility. Mobility can readily be measured, and the corresponding conductivity

15   can be approximated. Conductivity in a device comprising an aromatic organic semiconductor depends on the size and separation of crystal grains. The size distribution of crystal grains determines how many of them must be effectively traversed by a charge carrier in order to be transported from an origin to a destination such as between a source and drain, for example. The separation between crystal grains determines the impact of non-crystalline regions on

20   conductivity. For example, crystal grains separated by a distance greater than the maximum inter-grain tunneling distance for a particular semiconductor material may constitute a nonconductive pathway for charge carriers. Conductivity within a crystal grain of an organic semiconductor also depends on charge carrier energy levels and molecular overlaps in the crystal.

One aromatic organic semiconductor that can be used is tetracene. Tetracene is a linear

25   acene having four aromatic rings. Films of tetracene are capable of conductive transport by

holes. For example, a polycrystalline film of tetracene generally provides a low mobility, within a range between about 10^{-5} cm^2/Vs and about 0.01 cm^2/Vs at room temperature. In contrast, where crystallization of tetracene is promoted, mobilities within a range between about 0.1 cm^2/Vs and about 1 cm^2/Vs at room temperature can be achieved.

5   In one embodiment, monochlorotetracene is used as the aromatic organic semiconductor. The chlorine atom may, for example, be bonded to one of the interior benzene rings of the molecule. Tetracene is not readily dissolved in common solvents. The solubility of tetracene in methylene chloride is about 0.125 mg/ml; and the solubility of monochlorotetracene in methylene chloride is about 25 mg/ml. Hence, monochlorotetracene has a much higher

10   solubility, relatively about 200 times greater in methylene chloride for example, thus allowing for increased crystal formation from solution. Alternatively, tetracene having another substituent such as an alkyl or halogen moiety can be used. In general, non-aromatic substituents on aromatic semiconductor molecules disrupt pi-bonding and can be employed to thus decrease the ability of molecules to stack together in a lattice and to prematurely crystallize. In this

15   embodiment, the composition of the compound for the coating to constitute semiconductor crystal nucleation augmentation regions is selected to have an influential amount of pi-electrons. In one embodiment, the composition of the compound for the coating to constitute semiconductor crystal nucleation augmentation regions comprises a triphenyl group, in which, for example, the phenyl groups may be mutually para-bonded. In this embodiment, one of the phenyl groups in

20   the compound can include a thiol group to facilitate bonding of the compound to a gold substrate. For this purpose, for example, the coating compound for forming the semiconductor crystal nucleation augmentation regions may be a triphenylthiol. Further in this embodiment, one of the phenyl groups in the compound can include a SiCl$_3$ group or a SiOR$_3$ group to facilitate bonding to a dielectric layer comprising silicon. For this purpose, for example, the coating composition

25   for forming the semiconductor crystal nucleation augmentation regions may comprise

triphenyl-trichlorosilane or triphenyl-triethoxysilane. In another embodiment, anthracene is used as the aromatic organic semiconductor. In this embodiment, the composition of the compound for the coating to constitute semiconductor crystal nucleation augmentation regions is selected to have an influential amount of pi-electrons.

5   In the preceding embodiments regarding chlorotetracene and anthracene, the composition of the coating for forming the semiconductor crystal nucleation inhibition regions generally has a non-influential amount of pi-electrons. In one embodiment regarding chlorotetracene and anthracene, the composition of the coating for forming the semiconductor crystal nucleation inhibition regions comprises an exemplary compound comprising a moiety selected from the

10   group including: biphenyl, phenyl, alkane, carboxylic acid, fluorinated hydrocarbon, and propyl amine. Accordingly, exemplary compounds for use in coatings for forming the semiconductor crystal nucleation inhibition regions on gold electrodes include: biphenylthiol, benzylthiol, dodecanethiol, $NH_2-(CH_2)_3SH$ and $HOOC-(CH_2)_{11}-SH$. Further, exemplary compounds for use in coatings for forming the semiconductor crystal nucleation inhibition regions on a dielectric

15   layer comprising silicon include: biphenyl-trichlorosilane, biphenyl-triethoxysilane, phenyl-trichlorosilane, phenyl-triethoxysilane, dodecane-trichlorosilane, dodecane-triethoxysilane, $NH_2-(CH_2)_3Si-(OR)_3$, $HOOC-(CH_2)_{11}Si-(OR)_3$, $NH_2-(CH_2)_3Si-Cl_3$, and $HOOC-(CH_2)_{11}SiCl_3$.

It will be understood that the teachings herein likewise extend to other aromatic semiconductors and to mixed aromatic semiconductors. In further exemplary embodiments, a

20   bithiophene such as 5,5'-bis-(4-ethylphenyl)2,2'-bithiophene or 5,5'-bis-(8-hexylfluorine-1-yl)2,2'-bithiophene is employed as the semiconductor. In additional exemplary embodiments, a thiophene such as sexithiophene or a benzothiophene dimer is employed as the semiconductor. Further exemplary thiophene compounds that can be used include: 2,5-linked thiophene tetramers, pentamers, and hexamers, either unsubstituted or substituted at the terminal 5 positions

25   with linear alkyl or alkoxyalkyl chains of about 4 to about 12 atoms in length; anthradithiophene

and terminal dialkyl derivatives thereof, including for example dihexylanthradithiophene; regioregular poly (3-hexylthiophene); and co-oligomers of 2,5-linked thiophene rings and 1,4-linked benzene rings about 5 rings long, either unsubstituted or substituted as described for the thiophene oligomers, including for example 1,4-bis(5-(5-hexylthien-2-yl)thien-2-yl)benzene

5   (DHT4Ph). DHT4Ph can be synthesized according to procedures described for hexylated 5- and 6-ring compounds in W. Li et al, Chem. Mater., Vol. 11, page 458 (1999), the entirety of which is hereby incorporated herein, using 1,4-diiodobenzene as the source of the benzene ring. Other substituted and unsubstituted acenes such as anthracene, pentacene and hexacene for example, other bithiophenes, other thiophenes, phthalocyanines including for example copper

10   phthalocyanine and perfluorinated copper phthalocyanine, naphthalene-1,4,5,8-tetracarboxylic diimide compounds, naphthalene-1,4,5,8-tetracarboxylic dianhydride, and 11,11,12,12-tetracyanonaphtho-2,6-quinodimethane, for example, can also be used. See, for example, Dimitrakopoulos et al. U.S. Patent. No. 5,981,970, Bauntech, et al. U.S. Pat. No. 5,625,199, Garnier, et al. U.S. Patent No. 5,347,144, and Klauck, Hagen et al., "Deposition: Pentacene

15   organic thin-film transistors and ICs," Solid State Technology, Vol. 43, Issue 3, March 2, on pp. 63-75. The entirety of the foregoing patents and article cited in this paragraph are hereby incorporated herein by reference in their entirety.

Pentacene is a particularly desirable organic semiconductor, because single crystals can be made having mobilities within a range between about 1 cm^2/Vs and about 5 cm^2/Vs at room

20   temperature. However, pentacene is not readily dissolved in common solvents. In one embodiment, a pentacene derivative having enhanced solubility in a solvent, such as chloropentacene, is employed as the semiconductor. Further for example, tetramethylpentacene or tetraethylpentacene can be used. In another embodiment, a soluble pentacene precursor is employed as the semiconductor and later converted into pentacene itself. Pentacene precursors

25   are disclosed, for example, in Dimitrakopoulos et al. U.S. Patent. No. 5,981,970.

It will be understood that the teachings herein likewise extend to other coating compositions to constitute the semiconductor crystal nucleation augmentation regions. In one embodiment, the composition used to make the semiconductor nucleation augmentation regions comprises a compound comprising an aromatic moiety having at least three aromatic rings with

5   conjugated pi-bonding. In another embodiment, the compound comprising an aromatic moiety comprises at least three mutually connected benzene rings, with a thiol or reactive silicon-containing group as explained above, located at an extremity of the compound molecule. The benzene rings may either be mutually bridged through alkyl bonds, or fused. The benzene rings may either be mutually oriented in a straight chain and bonded through para positions, or may

10   include branching and non-para bonding. For example, oligo(para-phenylenes) such as para-terphenyl, para-quaterphenyl, para-pentaphenyl, and para-sexiphenyl can be used. Para-terphenyl and para-quaterphenyl are commercially available from Sigma-Aldrich. Para-sexiphenyl is commercially available from Tokyo Kasei Kogyo Co. Ltd. In further embodiments, non-aromatic regions may be interposed between the aromatic region of the

15   compound and the thiol or reactive silicon group. For example, a straight- or branched-chain hydrocarbon group that is saturated or unsaturated in whole or part, or also containing alicyclic moieties in whole or part, having between 0 and about 16 carbon atoms, can be so used. In further embodiments, a monothiolated acene or an acene comprising a reactive silicon group, and comprising at least three aromatic rings is employed as the aromatic compound. For example, the

20   acene may be anthracene, tetracene or pentacene. In further embodiments, benzene rings in the foregoing compounds are substituted in whole or part by other aromatic systems such as pyridine or pyrrole moieties. Desirably, the use of mixtures of compounds is avoided as typically they will not form ordered self-assembled monolayers.

It will be understood that the teachings herein likewise extend to other coating

25   compositions to constitute the semiconductor crystal nucleation inhibition regions. The

compound may comprise aliphatic or alicyclic moieties, for example, and the compound is designed so that the non-aromatic moieties interface with the subsequently applied aromatic semiconductor. In additional embodiments, the compound can comprise further hydrocarbon, heteroatom or other charged or uncharged moieties. For example, a straight- or branched-chain

5   hydrocarbon moiety that is saturated or unsaturated in whole or part, or also containing alicyclic moieties in whole or part, can be used. Alkane thiols and silanes having between 2 and 16 carbon atoms, for example, can be used. Exemplary compounds include undecylthiol, dodecylthiol, undecyl-trichlorosilane, and dodecyl-triethoxysilane. In one embodiment, the composition used to make the semiconductor nucleation inhibition regions comprises a charged

10   group to further decrease the affinity to the aromatic semiconductor. Desirably, such a charged group is positioned at or near a longitudinal end of the compound opposite to the longitudinal end where the thiol or reactive silicon group is located. In one embodiment, a negatively charged carboxylic acid, sulphonate or phosphonate group is so provided on the compound. In another embodiment, a positively charged amino group is so provided on the compound. In additional

15   embodiments, the compound can comprise further hydrocarbon, heteroatom or other charged or uncharged moieties. For example, the compound can be substituted by halogens such as fluorine, such as tridecafluoro-1,1,2,2-tetrahydro-octyl-triethoxysilane, or 4-mercapto-1-fluorobenzene.

In another embodiment, the coating composition to constitute the semiconductor crystal nucleation inhibition regions comprises a compound comprising a plurality of aromatic rings and

20   a thiol or reactive silicon group at one end, and comprising a non-aromatic group at the other end of sufficient mass to shield the aromatic semiconductor from aromatic pi-bonding interactions. In a further embodiment, the coating composition to constitute the semiconductor crystal nucleation inhibition regions comprises molecules of a compound that are deposited in a non-crystalline, random state on the substrate to be patterned.

General procedures for synthesizing thiol-terminated conjugated oligomers are

summarized in B. de Boer, H. Meng, D.F. Perepichka, J. Zheng, Y. Chabal, F. Wudl, P.G. Van

Patten, and Z. Bao, "Synthesis and Characterization of Conjugated Mono- and Dithiol Oligomers

and Characterization of Their Self-Assembled Monolayers", Langmuir, 19, pp. 4272-4284, 2003.

5   General procedures for synthesizing reactive-silicon - terminated compounds with aromatic ends

are summarized in Collet, J., et al., "High Anisotropic Conductivity in Organic Insulator /

Semiconductor Monolayer Heterostructure," Applied Physics Letters, Vol. 76, No. 10, pp. 1339-

1341, March 6, 2000. General procedures for synthesizing $SiCl_3$ and $SiOR_3$ compounds are

described in Fritz, G. and Matern, E., "Carbosilanes Synthesis and Reactions," Springer-Verlag,

10   New York, 1986. All of the foregoing documents are hereby incorporated herein in their

entirety.

In further embodiments, a dielectric layer comprising aluminum oxide is substituted for

the silicon-containing dielectric layers discussed above. In such embodiments, silane groups are

replaced by phosphonic acid groups in the compounds to be applied to create patterned regions of

15   semiconductor crystal nucleation augmentation regions and semiconductor nucleation inhibition

regions for bonding to the aluminum oxide substrate. In further embodiments, a dielectric layer

comprising another metal oxide is substituted for the silicon-containing dielectric layers

discussed above. In such embodiments, silane groups are replaced by carboxylic acid groups or -

CONHOH groups for bonding to the metal oxide substrate.

20   In one embodiment, thin film transistors 102 and 104 shown in Figs. 1 and 2 having

chlorotetracene polycrystalline semiconductor regions 140 and 142, respectively, are fabricated

by an exemplary method 700 shown in Fig. 7.

Referring to Fig. 7, at step 705 a silicon wafer is provided to serve as the supporting

substrate 146 shown in Fig. 2. The silicon wafer provides structural support for the transistors

25   102 and 104, and has an oxidized dielectric surface comprising silicon dioxide. In alternative

embodiments, a supporting substrate composed of other materials is used, or the supporting substrate 146 is omitted.

At step 710, the gate electrode 144 is applied to the supporting substrate 146. The gate electrode 144 can be applied by a variety of conventional methods, such as by sublimation of

5   elemental gold in a vacuum, by electrodeposition, or by electroless deposition. Silicon wafers having preapplied gate electrodes also are commercially available. In further embodiments, the gate electrode 144 is fabricated from another conductive metal such as, for example, silver, platinum, palladium, copper, or alloys of such elements.

At step 715, dielectric layer 110 is provided on the gate electrode 144. To produce the

10   dielectric layer 110, a precursor composition is applied to the gate electrode 144. For example, the selected precursor composition may be dissolved in a solvent and applied to the gate electrode 144 by surface-initiated growth, spin-coating or casting techniques. In the coating and casting techniques, the dielectric layer 110 is converted into a solid form, for example, by drying, polymerizing and/or curing of the selected coated or cast composition. The dielectric layer 110

15   may be fabricated from any dielectric precursor composition, such as an inorganic or organic composition. The dielectric precursor composition may comprise monomeric, oligomeric or polymeric organic materials, or inorganic materials, and blends of the same. The term "blends" as used in this specification broadly encompasses and includes copolymers formed from the corresponding monomers, oligomers, and polymers, mixtures of polymers, and other

20   compositions comprising the same as well as compositions comprising inorganic materials, however produced. In another embodiment, the dielectric precursor composition comprises an organic compound that is polymerizable to form a dielectric polymer, such as an imide, acrylate, methacrylate , isocyanate, epoxide, vinylsilane, silsesquioxane, cycloalkene or ethacrylate for example.

At step 720, gold source electrodes 106 and 112 and drain electrodes 108 and 114, are provided on the dielectric layer 110. For example, a steel shadow mask can be placed over the surface of the dielectric layer 110, leaving exposed those portions of the surface where the electrodes are to be located. In one embodiment, the gap between source electrode 106 and drain

5   electrode 108, and the gap between source electrode 112 and drain electrode 114, are designed to be as small as possible to facilitate bridged growth of single semiconductor crystals between them on regions 140 and 142. For example, such gaps may be less than about 5 microns in width. The partially formed transistors are then placed in a vacuum chamber such as a bell jar. A source of gold metal is also placed in the vacuum chamber and heated to vaporize and deposit

10   gold over the shadow mask to produce the source electrodes 106 and 112, and drain electrodes 108 and 114. Other materials for fabricating source and drain electrodes can be substituted for gold. For example, silver, platinum, palladium, copper, or alloys of such elements can be used.

At step 725, the exposed surfaces of the gold source electrodes 106 and 112 and drain electrodes 108 and 114 are thoroughly cleaned. For example, the electrodes can be subjected to

15   an aggressive cleaning solution such as a piranha solution. An exemplary piranha solution comprises a 2:1 mixture by volume of sulfuric acid (98% by volume, in water) and hydrogen peroxide (30% by volume, in water). Following exposure to the piranha solution for a moderate time, such as about 5 minutes, the electrodes are thoroughly washed in deionized ultrapure water. Other conventional methods for thoroughly cleaning the electrodes can also be employed.

20   At step 730, a first thiol compound is transferred to the source electrodes 106 and 112 and drain electrodes 108 and 114 by a soft lithography process. According to this process, an elastomeric stamp is prepared for transfer application of the first thiol compound to the source and drain electrodes. In one embodiment, such an elastomeric stamp is fabricated from polydimethyl siloxane (PDMS). For example, 10 parts of a silicone elastomer base can be

25   thoroughly mixed with one part of a silicone elastomer curing agent to form the stamp. In

alternative embodiments, other polymers such as polyurethanes can be used for the stamp. Further background is provided in Y. Xia and G.M. Whitesides, "Soft Lithography", Angew. Chem. Int. Ed. 1998, 37, pp. 550 - 575, which is hereby incorporated herein in its entirety.

Next, a silicon master wafer is provided having a raised surface that is patterned

5   corresponding to the desired positioning for regions on the source and drain electrodes that will be coated either by semiconductor crystal nucleation augmentation layers or semiconductor nucleation inhibition layers. Such a master wafer can be prepared, for example, by conventional photoresist masking and etching techniques. In alternative embodiments, master wafers composed of other materials can be used. The patterned surface of the silicon master wafer is

10   then treated with a release agent, such as by fluorination, for example. Such fluorination can be carried out by exposing the patterned surface to tridecafluoro-1,1,2,2-tetrahydrooctyl-tiethoxysilane. The exposure can be carried out for about 15 minutes in the gas phase. In alternative embodiments, other release agents can be used. The PDMS mixture is then poured onto the patterned surface of the silicon master wafer, and the master wafer is then placed in a

15   petri dish and dried in an oven at about 65 degrees centigrade (°C) for at least about 2 hours. The cured PDMS is then removed from the patterned silicon master wafer with a utility knife. See, for example, Y. Xia and G.M. Whitesides, "Soft Lithography", Angew. Chem. Int. Ed. 1998, 37, pp. 550 - 575. In alternative embodiments, other methods for applying the selected polymer to the master wafer in order to prepare a transfer stamp can be employed. For example, liquid film

20   casting, spin casting and evaporative film casting can be employed.

A first solution comprising a thiol terminated compound is then loaded onto the PDMS stamp. The first thiol solution can be designed either to generate semiconductor crystal nucleation augmentation regions 116-122, or to generate semiconductor nucleation inhibition regions 124-138. In one embodiment, the first thiol solution includes a solute that is designed to

25   generate semiconductor crystal nucleation augmentation regions 116-122. The solute is a

compound comprising an aromatic moiety and a thiol group as discussed above, such as (para-terphenyl)-para-thiol for example. In one embodiment, a 2 millimolar solution of (para-terphenyl)-para-thiol in methylene chloride is prepared. Cotton applicators are submerged in the (para-terphenyl)-para-thiol solution and wiped over the patterned surface of the PDMS stamp.

5   The PDMS stamp is then dried with a stream of nitrogen for at least about 1 minute. The PDMS stamp is then applied once to a receiving surface such as a gold substrate to remove excess (para-terphenyl)-para-thiol. Alternative methods for applying the first thiol to the PDMS stamp include vapor deposition, liquid film casting, and spin casting.

The PDMS stamp is then used to apply a patterned coating of the (para-terphenyl)-para-

10   thiol onto the source electrodes 106 and 112 and the drain electrodes 108 and 114, yielding the desired semiconductor crystal nucleation augmentation regions 116-122. The semiconductor crystal nucleation augmentation regions 116-122 are self-assembled monolayers ("SAM") of (para-terphenyl)-para-thiol molecules desirably having a thickness of one molecule on the source and drain electrodes. The SAM blocks further thiol bonding in the patterned areas on the source

15   and drain electrodes intended to constitute the semiconductor crystal nucleation augmentation regions 116-122. The patterned coating is permitted to remain undisturbed on the source and drain electrodes for at least about 5 minutes. Each such PDMS stamp can be used for several applications, such as about six applications for example. Background information is provided in Y. Xia and G.M. Whitesides, "Soft Lithography", Angew. Chem. Int. Ed. 1998, 37, pp. 550 -

20   575.

In alternative embodiments, a patterned coating of the first thiol is applied to the source electrodes 106 and 112 and the drain electrodes 108 and 114 by methods such as ink jet printing, photolithography, and processes involving direct or indirect transfers from a transfer sheet or web to a desired substrate.

At step 735, the source electrodes 106 and 112 and the drain electrodes 108 and 114 are rinsed and dried. For example, the source and drain electrodes can be rinsed twice with isopropanol and then dried for at least about 30 seconds with a stream of nitrogen.

At step 740, the source electrodes 106 and 112 and the drain electrodes 108 and 114 are
5   exposed to a second thiol. Where the first thiol is designed to generate semiconductor crystal nucleation augmentation regions 116-122, the second thiol is designed to generate semiconductor nucleation inhibition regions 124-138. In one embodiment, the second thiol solution is designed to generate semiconductor nucleation inhibition regions 124-138. In such an embodiment, the second thiol is a compound comprising a thiol group and an exemplary non-aromatic region as
10   discussed earlier, such as dodecylthiol. In one embodiment, a 2 millimolar solution of dodecylthiol in absolute ethanol is prepared. During step 740, the first thiol blocks further thiol bonding in the patterned areas intended to constitute the semiconductor crystal nucleation augmentation regions 116-122. Thus, the second thiol only bonds to the source electrodes 106 and 112 and the drain electrodes 108 and 114 in the remaining areas intended to constitute the
15   semiconductor nucleation inhibition regions 124-138. Accordingly, the source and drain electrodes can be simply immersed in the dodecylthiol solution for a moderate time period such as 30 minutes, to form the semiconductor nucleation inhibition regions 124-138. In one embodiment, the source and drain electrodes are so immersed by dipping them into and pulling them out of the dodecylthiol solution in a direction parallel to their longitudinal axes. The
20   semiconductor nucleation inhibition regions 124-138 are SAMs of dodecylthiol molecules desirably with a thickness of one molecule on the source and drain electrodes. The coatings are permitted to remain undisturbed on the source and drain electrodes for at least about 5 minutes. In alternative embodiments, the second thiol is applied to the source and drain electrodes by methods such as ink jet printing, photolithography, and processes involving direct or indirect
25   transfers from a transfer sheet or web to a desired substrate.

At step 745, the source electrodes 106 and 112 and the drain electrodes 108 and 114 are again rinsed and dried. For example, the source and drain electrodes can be rinsed twice with isopropanol and then dried for at least about 30 seconds with a stream of nitrogen.

At step 750, the source electrodes 106 and 112 and the drain electrodes 108 and 114 are

5 exposed to a solution of a selected aromatic organic semiconductor such as 5-chlorotetracene. In embodiments where a dip-coating method is used to deposit the organic semiconductor, 5-chlorotetracene may provide better solubility than tetracene, so that larger crystals can be made. In embodiments where nucleation is facilitated by soaking the source and drain electrodes in a solution saturated with organic semiconductor, either tetracene or 5-chlorotetracene can be used.

10 In one embodiment, the selected semiconductor is dissolved by a solvent to form a solution, which is then applied to the semiconductor crystal nucleation augmentation regions 116-122 and to the semiconductor nucleation inhibition regions 124-138 on the source electrodes 106 and 112 and the drain electrodes 108 and 114. For example, where the semiconductor is dissolved in solution, the surfaces of the source and drain electrodes can then be immersed in the

15 solution so that the semiconductor crystallizes out of the solution on the semiconductor crystal augmentation regions to grow a polycrystalline semiconductor. In this manner, semiconductor molecules can interact with the surfaces of the semiconductor crystal nucleation augmentation regions 116-122 until the solvent is removed, such as by evaporation. Deposition of the semiconductor depends on the ability of the regions 116-138 on the source electrodes 106 and

20 112 and the drain electrodes 108 and 114 to facilitate nucleation. The promoted nucleation over the semiconductor crystal nucleation augmentation regions 116-122 results in a formation of polycrystalline semiconductor regions 140 and 142, respectively. Nucleation of semiconductor crystals directly on the semiconductor crystal nucleation augmentation regions 116-122 leads to growth of such crystals also bridging the gap between source electrode 106 and drain electrode

25 108, as well as the gap between source electrode 112 and drain electrode 114. The inhibited

nucleation over semiconductor nucleation inhibition regions 124-138 results in small amounts of or no crystallization. In this manner, the semiconductor crystal nucleation augmentation regions 116-122 and the semiconductor nucleation inhibition regions 124-138 collectively direct the formation of patterned polycrystalline semiconductor regions 140 and 142.

5   Where a semiconductor solution is so employed, semiconductor molecules that initially contact one of the semiconductor nucleation inhibition regions 124-138 can flow across the electrode surface, and make contact with one of the semiconductor crystal nucleation augmentation regions 116-122. In this manner, the deposition of the crystalline semiconductor occurs on the desired semiconductor crystal nucleation augmentation regions 116-122 and does

10   not occur on the semiconductor nucleation inhibition regions 124-138. Dissolution of the semiconductor molecules in a solvent promotes the growth of large single semiconductor crystals from the initially formed nuclei. For example, single crystals may be formed having dimensions that span the source and drain electrodes of a thin film transistor.

In another embodiment, the selected semiconductor is applied in a vapor state to the

15   semiconductor crystal nucleation augmentation regions 116-122 and to the semiconductor nucleation inhibition regions 124-138. Vapor deposition is particularly desirable for use with semiconductor oligomers having low solubilities, such as pentacene. In order to avoid nonselective bonding of the semiconductor on contact with the source electrodes 106 and 112 and the drain electrodes 108 and 114, vapor state deposition of semiconductors is generally

20   carried out at a rate of less that 1 angstrom per second (Å/s), more preferably less than 0.5 Å/s and employing low concentrations of the semiconductor suspended in a gaseous vehicle. The vapor deposition rate is proportional to the semiconductor concentration and to the rate of flow of the gaseous suspension. Examples of the experimental details for vapor phase deposition can be found in: Forrest, S. R. Ultrathin Organic Films Grown by Organic Molecular Beam Deposition

25   and Related Techniques. Chem. Rev., Vol. 97, p. 1793 (1997), the entirety of which hereby is

incorporated herein by reference. In many cases, however, vapor deposition of an organic

semiconductor on a patterned surface may not result in well resolved patterned nucleation.

In one exemplary embodiment, monochlorotetracene semiconductor is dissolved in

methylene chloride:chloroform (4:1 by volume) and then applied by dip-coating to the

5   semiconductor crystal nucleation augmentation regions 116-122 and to the semiconductor

nucleation inhibition regions 124-138 on the source electrodes 106 and 112 and the drain

electrodes 108 and 114. Methylene chloride desirably has a relatively low boiling point to

facilitate its removal by evaporation. Other such solvents, such as tetrahydrofuran, can also be

used. In one embodiment, the monochlorotetracene is dissolved in methylene chloride to form a

10   1.1 milligram per milliliter (mg/ml) solution which is then filled into a quartz cuvette. The quartz

cuvette is housed in a sealed acrylic chamber to retain constant solvent vapor concentration at

room temperature. The partially formed transistors are then submerged in the

monochlorotetracene solution, and pulled out of the solution at a constant rate within a range

between about 0.01 millimeters per second (mm/sec) and about 0.1 mm/sec. In this manner,

15   semiconductor molecules can interact with the surfaces of the semiconductor crystal nucleation

augmentation regions 116-122 until the solvent is removed. The semiconductor crystal

nucleation augmentation regions 116-122 and the semiconductor nucleation inhibition regions

124-138 collectively direct the formation of patterned polycrystalline semiconductor regions 140

and 142. The semiconductor coating is permitted to remain undisturbed on the source electrodes

20   106 and 112 and the drain electrodes 108 and 114 for at least about 5 minutes.

In alternative embodiments, the selected semiconductor can be dissolved in other

solvents. In further alternative embodiments, other methods for applying the semiconductor may

be employed, such as liquid film casting, spin casting, or evaporative film casting.

At step 755, the completed transistors 102 and 104 are again rinsed and dried. For example, the transistors 102 and 104 can be rinsed twice with isopropanol and then dried for at least about 30 seconds with a stream of nitrogen in a nitrogen box.

In another embodiment, thin film transistors 302 and 304 shown in Figs. 3 and 4 having exemplary chlorotetracene polycrystalline semiconductor regions 316 and 318, respectively, are fabricated by an exemplary method 800 shown in Fig. 8.

Referring to Fig. 8, at step 805 a silicon wafer is provided in the same manner as discussed above in connection with step 705 of Fig. 7, to serve as the supporting substrate 324 shown in Fig. 4. At step 810, the gate electrode 322 is applied to the supporting substrate 324 in the same manner as discussed above in connection with step 710 of Fig. 7. Since thiol bonding is not used in this embodiment, however, the gate electrode, and the source and drain electrodes as further discussed below, can be fabricated if desired from other conductive metals and alloys, as well as conductive plastics and ceramics. At step 815, dielectric layer 310 is provided on the gate electrode 322 in the same manner as discussed above in connection with step 715 of Fig. 7. At step 820, gold source electrodes 306 and 312 and drain electrodes 308 and 314 are provided on the dielectric layer 310 in the same manner as discussed above in connection with step 720 of Fig. 7.

At step 825, a first compound containing reactive silicon atoms, such as $SiCl_3$ groups or $SiOR_3$ groups, is transferred to the dielectric layer 310 by a soft lithography process. According to this process, an elastomeric stamp is prepared in the same manner as discussed above in connection with step 730 of Fig. 7. A first solution comprising a compound containing reactive silicon atoms is then loaded onto the PDMS stamp. The first solution comprising a compound containing reactive silicon atoms can be designed either to generate semiconductor crystal nucleation augmentation regions 316 and 318 shown in Figs. 3 and 4, or to generate semiconductor nucleation inhibition regions 330, 332 and 334. In one embodiment, the first

solution comprises a compound containing reactive silicon atoms that is designed to generate

semiconductor crystal nucleation augmentation regions 316 and 318. The solute is a compound

comprising an aromatic moiety and a moiety containing reactive silicon atoms as discussed

above, such as (para-terphenyl)-para- $SiOR_3$.

5   In one embodiment, a precursor to a (para-terphenyl)-para- $SiOR_3$ compound is applied in

the desired pattern to form semiconductor crystal nucleation augmentation regions 316 and 318

and is then converted in situ to the (para-terphenyl)-para- $SiOR_3$ compound. In one embodiment,

a 2 millimolar solution of an alkene-$SiOR_3$ compound such as ethylene-triethoxysilane in

methylene chloride is prepared. Cotton applicators are submerged in the ethylene-triethoxysilane

10   solution and wiped over the patterned surface of the PDMS stamp. The PDMS stamp is then

dried with a stream of nitrogen for at least about 1 minute. The PDMS stamp is then applied

once to a receiving surface such as an SiO_2 wafer to remove excess ethylene-triethoxysilane.

Alternative methods for applying the first compound containing reactive silicon atoms to the

PDMS stamp include vapor deposition, liquid film casting, and spin casting.

15   The PDMS stamp is then used to apply a patterned coating of the ethylene-triethoxysilane

compound onto the dielectric layer 310, yielding precursors to the desired semiconductor crystal

nucleation augmentation regions 316 and 318. The terminal double bond of the ethylene moiety

in ethylene-triethoxysilane is subsequently converted first by oxidation into a —COOH moiety

and second into a —COCl moiety. The oxidation can be carried out, for example, by an aqueous

20   solution of $KMnO_4$ / $NaIO_4$ / K_2CO_3. The —COCl moiety is then allowed to react by

esterification at room temperature over an extended period such as 120 hours with an alcohol of

the formula R-OH, in which R is the desired aromatic moiety for interaction with the organic

semiconductor. A water trap can be used to enhance the reaction yield. For example, the alcohol

may be hydroxy-(para-terphenyl), so that the semiconductor crystal nucleation augmentation

25   regions 316 and 318 comprise (para-terphenyl)-para- $SiOR_3$. All of the precursor conversion

steps can be carried out by simply dipping the dielectric layer 310 into solutions of the

appropriate reagents followed by rinsing. The semiconductor crystal nucleation augmentation

regions 316 and 318 are self-assembled monolayers ("SAM") of (para-terphenyl)-para- $SiOR_3$

molecules desirably having a thickness of one molecule on the dielectric layer 310. One

5 advantage of such a procedure involving precursor application and conversion is that formation

of a more highly ordered layer of the exemplary (para-terphenyl)-para- $SiOR_3$ may be possible

than by direct application of such a compound. Alternatively, the exemplary (para-terphenyl)-

para- $SiOR_3$ may be synthesized by carrying out analogous reactions in solution. Background

information is provided in Collet, J., et al., "High Anisotropic Conductivity in Organic Insulator /

10 Semiconductor Monolayer Heterostructure," Applied Physics Letters, Vol. 76, No. 10, pp. 1339-

1341, March 6, 2000; and in Collet, J. et al., "Nano-Field Effect Transistor with an Organic Self-

Assembled Monolayer as Gate Insulator," Applied Physics Letters, Vol. 73, No. 18, pp. 2681-

2683, November 2, 1998, the entirety of both of which are hereby incorporated herein by

reference.

15   The SAM blocks further bonding of compounds comprising reactive silicon atoms in the

patterned areas on the dielectric layer 310 intended to constitute the semiconductor crystal

nucleation augmentation regions 316 and 318. The patterned coating is permitted to remain

undisturbed on the dielectric layer 310 for at least about 5 minutes. In alternative embodiments,

a patterned coating of the first compound comprising reactive silicon atoms is applied to the

20 dielectric layer 310 by methods such as ink jet printing, photolithography, and processes

involving direct or indirect transfers from a transfer sheet or web to a desired substrate.

        At step 830, the dielectric layer 310 is rinsed and dried. For example, the dielectric layer

310 can be rinsed twice with isopropanol and then dried for at least about 30 seconds with a

stream of nitrogen.

At step 835, the dielectric layer 310 is exposed to a second compound comprising reactive silicon atoms. Where the first compound comprising reactive silicon atoms is designed to generate semiconductor crystal nucleation augmentation regions 316 and 318, the second compound comprising reactive silicon atoms is designed to generate semiconductor nucleation

5 inhibition regions 330, 332 and 334. In one embodiment, the second solution comprising a compound comprising reactive silicon atoms is designed to generate semiconductor nucleation inhibition regions 330, 332 and 334. In such an embodiment, the second compound comprises reactive silicon atoms and a non-aromatic region as discussed earlier, such as dodecyl-$SiOR_3$. In one embodiment, a 2 millimolar solution of dodecyl- $SiOR_3$ in absolute ethanol is prepared.

10 During step 835, the first compound comprising reactive silicon atoms blocks further bonding of compounds comprising reactive silicon atoms in the patterned areas intended to constitute the .semiconductor crystal nucleation augmentation regions 316 and 318. Thus, the second compound comprising reactive silicon atoms only bonds to the dielectric layer 310 in the remaining areas intended to constitute the semiconductor nucleation inhibition regions 330, 332

15 and 334. Accordingly, the dielectric layer 310 can be simply immersed in the dodecyl- $SiOR_3$ solution for a moderate time period such as 30 minutes, to form the semiconductor nucleation inhibition regions 330, 332 and 334. The semiconductor nucleation inhibition regions 330, 332 and 334 are SAMs of dodecyl- $SiOR_3$ molecules desirably with a thickness of one molecule on the dielectric layer 310. The coatings are permitted to remain undisturbed on the dielectric layer

20 310 for at least about 5 minutes. In alternative embodiments, the second compound comprising reactive silicon atoms is applied to the dielectric layer 310 by methods such as ink jet printing, photolithography, and processes involving direct or indirect transfers from a transfer sheet or web to a desired substrate.

At step 840, the dielectric layer 310 is again rinsed and dried in the same manner as in

25 step 830.

At step 845, the dielectric layer 310 is exposed to a solution of a selected aromatic

organic semiconductor such as 5-chlorotetracene in the same manner as discussed above in

connection with step 750 of Fig. 7. The promoted nucleation over the semiconductor crystal

nucleation augmentation regions 316 and 318 results in a formation of polycrystalline

5   semiconductor regions 326 and 328, respectively. The inhibited nucleation over semiconductor

nucleation inhibition regions 330, 332 and 334 results there in small amounts of or no

crystallization. In this manner, the semiconductor crystal nucleation augmentation regions 316

and 318 and the semiconductor nucleation inhibition regions 330, 332 and 334 collectively direct

the formation of patterned polycrystalline semiconductor regions 326 and 328, which can include

10   single crystals having dimensions that span the source and drain electrodes of a thin film

transistor. At step 850, the completed transistors 302 and 304 are again rinsed and dried.

In another embodiment, thin film transistors 502 and 504 shown in Figs. 5 and 6 having

exemplary chlorotetracene polycrystalline semiconductor regions 510 and 516, respectively, are

fabricated by an exemplary method 900 shown in Fig. 9.

15   Referring to Fig. 9, at step 905 a silicon wafer is provided in the same manner as

discussed above in connection with step 805 of Fig. 8, to serve as the supporting substrate 534

shown in Fig. 6. At step 910, the gate electrode 532 is applied to the supporting substrate 534 in

the same manner as discussed above in connection with step 810 of Fig. 8. At step 915,

dielectric layer 518 is provided on the gate electrode 532 in the same manner as discussed above

20   in connection with step 815 of Fig. 8. At step 920, a first compound containing reactive silicon

atoms, such as $SiCl_3$ groups or $SiOR_3$ groups, is transferred to the dielectric layer 518, generally

in the same manner as discussed above in connection with step 825 of Fig. 8. In one

embodiment, the first such compound is tridecafluoro-1,1,2,2-tetrahydro-octyl-triethoxysilane,

commercially available from Gelest, Tullytown, Pennsylvania. The tridecafluoro-1,1,2,2-

25   tetrahydro-octyl-triethoxysilane is dissolved in ethanol to form a 1% solution by weight, and the

PDMS stamp holding this solution is placed in contact with the dielectric layer 518 for about 2

minutes. At step 925, the dielectric layer 518 is rinsed and dried generally in the same manner as

discussed above in connection with step 830 of Fig. 8, by baking at 130°C for about 30 minutes,

rinsing with 2-propanol, and drying with nitrogen gas for about 30 seconds. At step 930, the

5   dielectric layer 518 is exposed to a second compound comprising reactive silicon atoms in the

same manner as discussed above in connection with step 835 of Fig. 8. At step 935, the

dielectric layer 518 is again rinsed and dried in the same manner as in step 925. At step 940, the

dielectric layer 518 is exposed to a solution of a selected aromatic organic semiconductor such as

5-chlorotetracene in the same manner as discussed above in connection with step 845 of Fig. 8.

10   The promoted nucleation over the semiconductor crystal nucleation augmentation regions 520

and 522 results in a formation of polycrystalline semiconductor regions 510 and 516,

respectively. At step 945, the partially formed transistors 502 and 504 are again rinsed and dried

in the same manner as discussed above in connection with step 925. At step 950, gold source and

drain electrodes 506 and 508 are provided on semiconductor layer 510, and gold source and drain

15   electrodes 512 and 514 are provided on semiconductor layer 516, in the same manner as

discussed above in connection with step 820 of Fig. 8.

Figs. 7-9 as discussed above relate to exemplary and non-limiting embodiments of

methods that can be used . Other methods for making the exemplary devices shown in Figs. 1-6

can also be used.

20   In one embodiment, microcontact printing (μCP) was used to pattern metal surfaces with

different SAMs in order to selectively grow single crystals of semiconductor molecules and thus

simulate transistor fabrication. All solvents and chemicals were of reagent grade and used as

received unless otherwise stated. Methylene chloride, analytical grade potassium hydroxide,

absolute ethanol, isopropanol, hydrogen peroxide (30% by weight in water), H_2SO_4 (95.8% in

25   water), anthracene, tetracene, and tetrahydrofuran were all purchased from Sigma-Aldrich

Chemicals (Milwaukee, WI). Polydimethyl siloxane (PDMS) was purchased from Dow Corning

Corporation (Midland, MI). The compound 1-mercaptododecane was purchased from Alfa

Aesar Co. The compounds triphenylthiol and biphenylthiol were synthesized using the

procedures described in B. de Boer, H. Meng, D.F. Perepichka, J. Zheng, Y. Chabal, F. Wudl,

5   P.G. Van Patten, and Z. Bao, "Synthesis and Characterization of Conjugated Mono- and Dithiol

Oligomers and Characterization of Their Self-Assembled Monolayers", Langmuir, 19, pp. 4272-

4284, (2003), which is hereby incorporated herein in its entirety. Trifluoroethanethiol,

benzenethiol, NH_2-$(CH_2)_3$-SH, and COOH-$(CH_2)_{11}$SH were all purchased from Sigma-Aldrich

Chemicals. All aqueous solutions were prepared with doubly distilled water.

10   Thin gold film substrates for adsorption of SAMs were prepared by sputtering 30

nanometers (nm) of gold with a 1 nm-thick underlayer of titanium onto silicon wafers. The gold

substrates were then cleaned with a piranha solution and rinsed with water, acetone, and

isopropanol.

PDMS stamps were prepared by mixing 10 parts of silicon elastomer base to one part of

15   silicone elastomer curing agent. After thorough mixing of the two components, the PDMS

mixture was carefully poured over a patterned silicon wafer "master" that was placed in a plastic

Petri dish and dried in an oven at 65°C for at least about 2 hours. The patterned silicon master

was pretreated before application of the PDMS with a fluorinating silane for 15 minutes in the

gas phase, to facilitate peeling of the cured PDMS off of the silicon wafer master after drying in

20   the oven. After 2 hours of heat treatment, the PDMS was carefully removed from the patterned

silicon master with a utility knife. The dimensions of the patterned squares of the PDMS relief

stamp were 100 micrometers (μm) x 100 μm, the squares being mutually separated by 200 um.

Thiol-covered PDMS stamps were prepared by submerging cotton applicators into 2 millimolar

(mM) thiol solutions and wiping the applicators across the PDMS stamp. The PDMS stamps

25   were then dried with a stream of N_2 gas for at least about 1 minute to blow off excess thiol

molecules. Up to 6 stampings were carried out with each SAM coating onto the PDMS. However, the first stamping was not used to avoid cross over of excess thiol onto the non-stamped regions.

The compounds mercaptododecane, NH_2-$(CH_2)_3SH$, and $COOH$-$(CH_2)_{11}SH$ were

5   prepared in 2 mM concentrations in absolute ethanol. Methylene chloride was used to prepare 2 mM solutions of triphenylthiol, biphenylthiol and benzylthiol. Gold-coated silicon wafers were cut into rectangular pieces having dimensions of about 1 x 2 centimeters (cm) and treated with a piranha solution for 5 minutes. Next, the PDMS stamp was loaded with one of the thiols and carefully "wetted" onto the gold substrate. Background information is provided in Y. Xia and

10   G.M. Whitesides, "Soft Lithography", Angew. Chem. Int. Ed. 1998, 37, pp. 550 - 575.), the entirety of which hereby is incorporated herein by reference. The substrate was then rinsed twice with isopropanol and dried under a stream of N_2 gas. The substrate was immediately used in a dip coater to expose the thiol-treated surface to a selected aromatic organic semiconductor. The SAM-patterned gold substrates were submerged into a quartz cuvette filled with a 3 mM solution

15   of anthracene or tetracene. Methylene chloride was used as the solvent to dissolve the semiconductors. The substrates were soaked in the saturated solution of anthracene or tetracene for about 24 hours with a slow evaporation of the solvent and then pulled from the solution at a constant rate of between about 10 μm/second and about 100 μm/second. About 1 ml of solvent per 12 hours was evaporated per 5 ml of solution. The dip-coater was enclosed in a sealed

20   acrylic chamber to retain constant humidity at room temperature. Samples were immediately placed in a nitrogen box after single-crystal patterning.

Table 1 shows the percent surface coverage of anthracene and tetracene crystals formed onto different SAMs

SAM Type	Anthracene (%)	Tetracene (%)
triphenylthiol	23.0	4.7
biphenylthiol	6.3	NO GROWTH
Benzylthiol	3.2	NO GROWTH
mercaptododecane	1.0	NO GROWTH
$HOOC-(CH_2)_{11}SH$	2.4	NO GROWTH
$HS(CH_2)_3NH_2$	1.9	NO GROWTH

Table 1. Percent surface coverage of anthracene/tetracene crystals from different SAMs.

The data show that the crystals preferentially grew onto the triphenylthiol modified surfaces compared to the other SAMs. The percent surface coverage of the crystals decreased

5   with decreased aromatic ring moieties in the SAMs. Crystal growth onto non-aromatic SAMs produced about 90% less surface coverage than on the triphenylthiol SAM. There was 23% crystal growth for anthracene with a triphenylthiol SAM. However, there was only a 4.7% crystal growth for tetracene with a triphenylthiol passivated surface and no growth was observed with tetracene for the other SAMs.

10   Table 2 shows the surface coverage of the aromatic SAMs onto gold electrodes. There was more crystal growth onto surfaces that were least passivated. For example, triphenylthiol SAMs had a surface coverage of 1.93×10^{-10} moles per square centimeter (cm^2) compared to a surface coverage of 2.35×10^{-10} moles per cm^2 for benzenethiol, although there was approximately 7 times more crystal growth for surface prepared with triphenylthiol SAMs.

15

SAM Type	Moles/cm^2
triphenylthiol	1.93×10^{-10}
biphenylthiol	2.23×10^{-10}
Benzylthiol	2.35×10^{-10}

Table 2. Surface coverage of SAM onto gold substrates.

The monochlorotetracene crystal growth study was then extended to the patterning of gold substrates with two different SAMs. One SAM comprising a phenylthiol was used to induce crystal growth, while the other comprising dodecylthiol or 2,2,2-Trifluoroethanethiol inhibited crystal growth. Monochlorotetracene crystals nucleated and subsequently grew only on triphenylthiol SAMs and not on biphenylthiol or phenylthiol SAMs. It is theorized that the strong pi-pi interaction between the oriented triphenylthiol monolayer and the semiconducting molecule reduced the interfacial energy between their surfaces and therefore decreased the induction time for the nucleation of the semiconductor on the triphenylthiol SAM. This resulted in the selective nucleation at the triphenylthiol regions and in the subsequent depletion of the less active SAMs. See J. Aizenberg, A. J. Black & G. M. Whitesides, "Control of nucleation by patterned self-assembled monolayers," Nature Vol. 398, pp. 495-498 (1999), the entirety of which is hereby incorporated herein by reference. Fig. 10 shows a substrate stamped with triphenylthiol and soaked into a mercaptododecane SAM, prior to nucleation of monochlorotetracene. The 100 μm^2 squares are composed of semiconductor monochlorotetracene (MCT) crystals that were grown by the dip-coating method.

The compound 5-chlorotetracene was synthesized as follows. All chemicals were purchased from Sigma-Aldrich Chemical Co. and used without further purification. The reaction apparatus was flame-dried and the reactions were carried out under a nitrogen atmosphere. NMR (^{1}H and ^{13}C) spectra were recorded on a Bruker 360 MHz spectrometer and chemical shifts were

measured relative to trimethylsilane in $CDCl_3$ as solvent unless otherwise noted. Elemental

analysis was performed by Roberson Microlit Laboratories, Madison, NJ. Melting points were

uncorrected. Flash column chromatography was carried out on flash silica (Aldrich, 200-400

mesh). Anhydrous copper chloride ($CuCl_2$, 1.77 g, 13.2 mmol) and tetracene (3 g, 13.2 mmol)

5   were placed in a flask containing chlorobenzene (100 mL) under N_2. The mixture was stirred at

100 °C for 3 hours. After toluene (50 mL) was added, the resulting mixture was filtered to

remove unreacted copper chloride and the solvents were removed by rotary evaporation. The

solid residue was chromatographed with CH_2Cl_2:hexane (1:10 volume/volume) and subsequently

recrystallized from $CHCl_3$:methanol (3:1 volume/volume) to afford platelet-shaped crystals (1.20

10   g, 34.8%). mp 182 °C. ^1H NMR δ 7.43 (m, ^3H), 7.52 (t, ^1H), 7.98 (t, ^2H), 8.07 (d, ^1H), 8.47 (d,

^1H), 8.62 (s, ^1H), 8.65 (s, ^1H), 9.12 (s, ^1H). Elemental analysis results: C, 82.16; H, 4.21; Cl,

13.38. Calculated for $C_{18}H_{11}Cl$: C, 82.29; H, 4.22; Cl, 13.49.

In one embodiment, given a voltage of -50V from source to drain across a test transistor,

the charge carrier mobility of the semiconductor on the semiconductor crystal nucleation

15   augmentation regions is desirably at least about 10^{-3} cm^2/Vs, preferably at least about 10^{-2}

cm^2/Vs, and more preferably at least about 0.1 cm^2/Vs, at room temperature. The structure of the

semiconductor regions on the semiconductor crystal nucleation augmentation regions desirably

has an average crystal grain size of at least about 100 nanometers, and the grains desirably are

connected in the high mobility region. In one embodiment, the semiconductor nucleation

20   inhibition regions are characterized by low surface coverage of crystal grains, preferably no

crystal growths, and the grains are disconnected leading to no conduction paths. In one

embodiment, the mobility on the semiconductor nucleation inhibition regions is desirably within

a range between about 0 cm^2/Vs and about 10^{-4} cm^2/Vs at room temperature. In one

embodiment, the mobility of the semiconductor on the semiconductor crystal nucleation

augmentation regions is at least about 10 times as large as the mobility on the semiconductor nucleation inhibition regions.

While the present invention has been disclosed in the context of various aspects of presently preferred embodiments, it will be recognized that the invention may be applied to other environments consistent with the claims which follow.